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ART UNIT	**PAPER NUMBER**
2123	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/674,223	LAM ET AL.	
	Examiner	Art Unit	
	Russ Guill	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office action is a first action on the merits. Claims 1 - 20 have been examined. Claims 1 - 20 have been rejected.

Specification

2. The disclosure is objected to because of the following minor informalities:

a. In paragraph [0028], the specification recites, "a complied RTL design". This appears to be a minor grammatical error.

b. In paragraph [0034], the specification recites, "the state elements in the RTL are identifying by identifying". This appears to be a minor grammatical error.

c. In paragraph [0044], the specification recites, "the internal system call retrieve the requested information". This appears to be a minor grammatical error.

Claim Objections

3. Claim 11 is objected to because of the following informalities: The claim recites, "a resistor transfer level design".

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

a. **Claims 1 - 18 and 20** are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. One reasonably skilled in the art could not make or use the invention from the disclosure in the specification, coupled with information known in the art, without undue experimentation, for the following reasons:

i. Regarding claim 1 and dependent claims, the claim recites in lines 6 - 7, "modifying the programming language interface system call to reference the target in the first modified simulation design". This operation does not appear to be reasonably taught in the specification.

ii. Regarding claim 10 and dependent claims, the claim recites in lines 11 - 12, "modifying the programming language interface system call to reference the target in the first modified simulation design". This operation does not appear to be reasonably taught in the specification.

iii. Regarding claim 20, the claim recites in lines 6 - 7, "modifying the programming language interface system call to reference the target in the first modified simulation design". This operation does not appear to be reasonably taught in the specification.

iv. Regarding claim 4, the claim recites encoding the influenced set of relationships by obtaining values for high-level state elements and storing the high-level state element values in an array. The specification appears to teach that relationships are equivalent/corresponding state elements between the high-level design and the RTL design (*paragraph [0033]*). The

specification does not appear to teach that the relationships are encoded as values in an array.

v. Regarding claim 13, the claim is rejected as described in claim 4 above.

vi. Regarding claim 5, the limitation does not appear to be taught in the specification. It appears that the high-level state element values need to be obtained before the second modified hardware-level design is verified.

vii. Regarding claim 14, the limitation does not appear to be taught in the specification. It appears that the high-level state element values need to be obtained before the second modified hardware-level design is verified.

viii. Regarding claims 6 and 15, the specification does not appear to teach that a hardware state element may be a processor register or a memory.

ix. Regarding claims 7 and 16, the specification does not appear to teach that a high-level state element may be flip-flop or latch.

x. Regarding claim 8, the specification does not appear to teach the limitation. Especially, a relationship appears to mean an equivalent/corresponding state element in a high-level design and an RTL design (*paragraph [0033]*), but there is no teaching of one-to-one relationship, one-to-many relationship, or a mathematical function relationship.

xi. Regarding claim 17, the specification does not appear to teach the limitation. Especially, a relationship appears to mean an equivalent/corresponding state element in a high-level design and an RTL design (*paragraph [0033]*), but there is no teaching of one-to-one relationship, one-to-many relationship, or a mathematical function relationship.

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

a. Claims 1 - 20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

i. Regarding claim 1 and dependent claims, the claim recites in lines 4 – 5, "encoding a target of the programming language interface system call into the simulation design". It is unclear what "a target of the programming language interface system call" is. A claim interpretation would require considerable speculation and assumptions about the scope of the claim, and thus, a claim interpretation is not made. Further, the specification appears to teach that the values of high-level design state elements are encoded in the PLI, not in the simulation design (*paragraph [0040], "the values of the high-level design state elements corresponding to the remaining relationships are encoded in the PLI using arrays"*). Further, the following limitation references the target, but it is unclear what the target is.

ii. Regarding claim 10 and dependent claims, the claim recites in lines 9 - 10, "encoding a target of the programming language interface system call into the simulation design". It is unclear what "a target of the programming language interface system call" is. A claim interpretation would require considerable speculation and assumptions about the scope of the claim, and thus, a claim interpretation is not made. Further, the specification appears to teach that the values of high-level design state elements are encoded in the PLI, not in the simulation design (*paragraph [0040], "the values of the high-level design state elements corresponding to the remaining relationships are encoded in the PLI using arrays"*). Further, the following limitation references the target, but it is unclear what the target is.

iii. Regarding claim 19, the claim recites in line 2 - 3, "an encoded target of a programming language interface system call". The meaning of "an encoded target of a programming language interface system call" is unclear. A claim interpretation would require considerable speculation and assumptions about the scope of the claim, and thus, a claim interpretation is not made. Further, the specification appears to teach that the values of high-level design state elements are encoded in the PLI, not in the simulation design (*paragraph [0040], "the values of the high-level design state elements corresponding to the remaining relationships are encoded in the PLI using arrays"*). Further, the following limitation references the target, but it is unclear what the target is.

iv. Regarding claim 20, the claim recites in lines 4 - 5, "encoding a target of the programming language interface system call into the simulation design". It is unclear what "a target of the programming

language interface system call" is. A claim interpretation would require considerable speculation and assumptions about the scope of the claim, and thus, a claim interpretation is not made. Further, the specification appears to teach that the values of high-level design state elements are encoded in the PLI, not in the simulation design (*paragraph [0040], "the values of the high-level design state elements corresponding to the remaining relationships are encoded in the PLI using arrays"*). Further, the following limitation references the target, but it is unclear what the target is.

v. Regarding claims 9 and 18, the claims recite, "the second modified hardware-level design". The term appears to have insufficient antecedent basis. For the purpose of claim examination, the phrase is interpreted as, "the second modified simulation design".

Claim Rejections - 35 USC § 101

6. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

7. Claims 1 – 20 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

a. Regarding claim 19, the recited system appears to be entirely a software system, which is at best functional descriptive material *per se*, and thus is non-statutory. None of the claim limitations appear to expressly or inherently require tangible physical components. An ordinary artisan interpreting the claim in light of the specification would reasonably interpret the claim as encompassing a purely software system.

b. Regarding claim 1, the recited method appears to contain abstract ideas such as verifying the second modified simulation design. Therefore, to be statutory, the claim must be directed to a practical application producing a concrete, useful and tangible result. The claim does not appear to produce a tangible result needed to support a practical application. The result of the claim appears to be verifying the second modified simulation design, which does not appear to be a tangible result.

c. Regarding claim 10, the recited computer system appears to contain abstract ideas such as verifying the second modified simulation design. Therefore, to be statutory, the claim must be directed to a practical application producing a concrete, useful and tangible result. The claim does not appear to produce a tangible result needed to support a practical application. The result of the claim appears to be verifying the second modified simulation design, which does not appear to be a tangible result. While the computer system is tangible, the computer system does not appear to produce a tangible result.

d. Regarding claim 20, the recited apparatus appears to contain abstract ideas such as verifying the second modified simulation design. Therefore, to be statutory, the claim must be directed to a practical application producing a concrete, useful and tangible result. The claim does not appear to produce a tangible result needed to support a practical application. The result of the claim appears to be verifying the second modified simulation design, which does not appear to be a tangible result. While the apparatus may be tangible, the apparatus does not appear to produce a tangible result.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

10. **The claims have been rejected above under 35 USC § 112, second paragraph, as vague and indefinite. A claim interpretation would require considerable speculation about the meaning of terms employed in a claim or assumptions that must be made as to the scope of the claims. Therefore, a claim interpretation is not made, and the claims are treated below as best understood by the Examiner.**

11. **Claims 1 - 2, 9 - 11, 18 - 20** are rejected under 35 U.S.C. 103(a) as being unpatentable over Yim (Jooseo Yim et al., "Design Verification of Complex Microprocessors", 1996, Proceedings of IEEE Asia Pacific Conference on Circuits and Systems, pages 441 - 448)

in view of Fischer (Charles N. Fischer et al., "Crafting a compiler with C", 1991, Benjamin/Cummings Publishing Company, pages 622 - 636).

a. The art of Yim is directed to design verification of complex microprocessors, including verification of an RTL processor model by using an instruction set simulator in C (Polaris).

b. The art of Fischer is directed to using the C language to build a compiler, including methods of optimizing the compiler results.

c. The art of Yim and the art of Fischer are analogous art because they both include the use of the C programming language.

d. Regarding **claims 1, 20**:

e. Yim appears to teach:

f. obtaining the simulation design comprising a programming language interface system call (*page 444, figure 6, Verilog XL Simulator and Programming Language Interface, section F. Consistency Check, first and second paragraphs; page 443, figure 4*);

g. verifying the ~~second modified~~ simulation design using a simulation testbench (*page 444, figure 6, Verilog XL Simulator and Programming Language Interface, section F. Consistency Check, first and second paragraphs; page 443, figure 4, Co-simulation environment*).

h. Yim does not specifically teach:

i. encoding a target of the programming language interface system call into the simulation design to obtain a first modified simulation design;

j. modifying the programming language interface system call to reference the target in the first modified simulation design to obtain a second modified simulation design; and

k. ~~verifying the~~ second modified ~~simulation design using a simulation testbench~~.

l. Fischer appears to teach:

m. encoding a target of the programming language interface system call into the ~~simulation~~ design to obtain a first modified ~~simulation~~ design (*page 622, section 16.2.1 Inline Expansion of Subprogram Calls, first and second paragraphs*);

n. modifying the programming language interface system call to reference the target in the first modified ~~simulation~~ design to obtain a second modified ~~simulation~~ design (*page 622, section 16.2.1 Inline Expansion of Subprogram Calls, first and second paragraphs*);

o. The motivation to use the art of Fischer with the art of Yim would have been the benefit recited in Fischer that inline expansion of a subprogram call saves much of the overhead associated with calls (*page 622, section 16.2.1 Inline Expansion of Subprogram Calls, second paragraph*). Further motivation to use the optimization methods of Fischer would have been the problem recited in Yim that calling out of an RTL simulation results in a 10 - 20% speed degradation (*Yim, page 444, section F. Consistency Check, second paragraph*), which would have motivated the ordinary artisan to use optimization methods to reduce the speed degradation.

p. Obviousness must be determined in light of the knowledge of the ordinary artisan. Following are references that teach knowledge of the ordinary artisan:

i. Synopsys, "Smart Verification with VCS 7.0", April 2003, retrieved from www.synopsys.com/products/simulation/smart_verif_wp.html, pages 1 - 5; teaches using direct interface function calls to C (from Verilog) in order to achieve better performance than using programming language interface (*page 3, last paragraph*).

ii. Samir Palnitkar, "Verilog HDL", 1996, SunSoft Press, pages 157 - 167, 229 - 237, 249 - 251; teaches encoding values of state variables, and teaches PLI, and teaches Verilog internal function building.

iii. Ishtiaq (U.S. Patent Application Number 2004/0167766); teaches using a high-level processor model (including an instruction set simulator) in combination with a detailed model, such as a processor pipeline model, to produce accurate results. The invention recognizes that when modeling a device, it is common for the same execution path to be followed a large number of times in the same or similar circumstances. Thus, in order to speed the execution of the combined high-level model and detailed model, the invention stores during runtime a previously determined behavioral characteristic for a path as generated by the second model, and uses the previously stored characteristic when the same path is encountered (*paragraphs [0005] - [0011], [0013]*).

iv. Nathan Dohm et al., "Zen and the Art of Alpha Verification", 1998, Proceedings of International Conference on Computer Design: VLSI in Computers and Processors, seven unnumbered pages; teaches running an RTL model of the Alpha processor in lockstep with the Alpha instruction set simulator. Any discrepancies between the RTL and the ISS would immediately flag an error (*first page, right-side column, second paragraph*).

v. Marines Puig-Medina et al., "Verification of Configurable Processor Cores", 2000, Proceedings of the 2000 Design Automation Conference, pages 426 - 431; teaches an RTL processor model running in parallel with an instruction set simulator, and comparing states after instruction execution. A state mismatch causes the simulation to fail immediately (*page 428, section 3.2 Co-simulation (Cosim)*).

vi. Darren Brown et al., "Functional Verification of a Multiple-Issue, Out-of-Order, Superscalar Alpha Processor- The DEC Alpha 21264 Microprocessor", 1998, Proceedings of the Design Automation Conference 1998, pages 638 - 643; teaches running an RTL model of a processor with an instruction set processor, and comparing the states at run-time (*page 639, section 2, and figure 1*).

vii. Cox (U.S. Patent 5,991,529) teaches inputting a test to a device and comparing the output results with expected results (*column 4, lines 39 - 55*).

q. Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use the art of Fischer with the art of Yim to produce the claimed invention.

r. Regarding **claim 10**:

s. Most of claim 10 is taught as in claim 1 above. The difference is taught below.

t. Yim appears to teach:

u. A processor (*page 443, figure 3, Host Computer*);

v. a memory (*page 443, figure 3, Host Computer*);

w. a storage device (*page 443, figure 3, Host Computer*);

X. software instructions stored in the memory for enabling the computer system to perform (*page 443, figure 3, Host Computer*);

y. Regarding **claim 19**:

z. Yim appears to teach:

aa. a simulation design comprising a component (*page 443, section D. RTL StreC Model*), ~~an encoded target of a programming language interface system call, and a reference to the encoded target~~;

bb. a test vector providing an input signal value for the component in the simulation design (*page 444, figure 6, Verilog XL Simulator and Programming Language Interface, section F. Consistency Check, first and second paragraphs; page 443, figure 4*);

cc. a simulation testbench providing functionality to verify the simulation design using the test vector (*page 444, figure 6, Verilog XL Simulator and Programming Language Interface, section F. Consistency Check, first and second paragraphs; page 443, figure 4, Co-simulation environment*).

dd. Yim does not specifically teach:

ee. ~~a simulation design comprising a component~~, an encoded target of a programming language interface system call, and a reference to the encoded target.

ff. Fischer appears to teach:

gg. an encoded target of a programming language interface system call, and a reference to the encoded target (*page 622, section 16.2.1 Inline Expansion of Subprogram Calls, first and second paragraphs*).

hh. Regarding **claims 2, 11**:

ii. Yim appears to teach:

jj. the simulation design comprises a register transfer level design (*page 443, section D. StreC: RTL C model, and page 444, section F. Consistency Check*).

kk. Regarding **claims 9, 18**:

ll. A second modified hardware-level design is taught as in claims 1 and 10 above. The difference is taught below.

mm. Yim appears to teach:

nn. the ~~second modified hardware level~~ design is verified on a hardware-based simulation test bench (*page 443, section E. Gate-level Verilog Simulation with hardware accelerator, and figure 6*).

12. **Claims 3 - 7 and 12 - 16** are rejected under 35 U.S.C. 103(a) as being unpatentable over Yim as modified by Fischer as applied to claims **1 - 2, 9 - 11, 18 - 20** above, further in view of Ishtiaq (U.S. Patent Application Number 2004/0167766).

a. The art of Yim as modified by Fischer teaches a method for providing verification of a simulation design as recited in claims **1 - 2, 9 - 11, 18 - 20** above.

b. The art of Ishtiaq is directed to modeling device behavior using a first model, a second model and stored valid behavior (*Title*).

c. The art of Ishtiaq and the art of Yim as modified by Fischer are analogous art because both Yim and Ishtiaq are concerned with running a detail model and a behavioral model in parallel, and obtaining run-time results by one model from the other model.

d. Regarding **claims 3, 12:**

e. Yim appears to teach:

f. obtaining a set of hardware state elements from the simulation design (*page 444, section F. Consistency Check, second paragraph; since StreC and MCV run in parallel and immediately compare state results, the limitation would have been obvious*);

g. obtaining a set of high-level state elements from a high-level design (*page 444, section F. Consistency Check, second paragraph; since StreC and MCV run in parallel and immediately compare state results, the limitation would have been obvious*);

h. determining a common set of state elements from the set of hardware state elements and the **set** of high-level state elements (*page 444, section F. Consistency Check, second paragraph; since StreC and MCV run in parallel and immediately compare state results, the limitation would have been obvious*);

i. identifying at least one relationship between the high-level state element and the hardware state element in the common set of state elements (*page 444, section F. Consistency Check, second paragraph; since StreC and MCV run in parallel and immediately compare state results, the limitation would have been obvious*);

j. determining whether the at least one relationship is influenced by the test vector to obtain an influenced set of relationships (*page 444, section F. Consistency Check, second paragraph; since StreC and MCV run in parallel and immediately compare state results, the limitation would have been obvious*);

k. Yim does not specifically teach:

l. encoding the influenced set of relationships to obtain a modified simulation design.

m. Ishtiaq appears to teach:

n. encoding the influenced set of relationships to obtain a modified simulation design (*paragraphs [0005] - [0013]; since the values from one model are saved for future use, the limitation would have been obvious*).

o. The motivation to use the art of Ishtiaq with the art of Yim as modified by Fischer would have been the benefit recited in Ishtiaq that the modeling process will gradually speed up as valid stored results enable a call to be omitted (*paragraph [0011]*).

p. Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use the art of Ishtiaq with the art of Yim as modified by Fischer to produce the claimed invention.

q. Regarding **claims 4, 13**:

r. Yim appears to teach:

s. obtaining high-level state element values for the high-level state elements in the influenced set of relationships from a simulation of the high-level design (*page 444, figure 6, Verilog XL Simulator and Programming Language Interface, section F. Consistency Check, first and second paragraphs; page 443, figure 4*);

t. Yim does not specifically teach:

u. storing the high-level state element values in an array.

v. Ishtiaq appears to teach:

w. storing the high-level state element values in an array (*paragraphs [0005]-[0013]*).

x. Regarding **claims 5, 14**:

y. Yim appears to teach:

z. the high-level state element values are obtained during concurrent execution of a high-level design simulation and verification of the second modified hardware-level design (*page 444, section F. Consistency Check, first and second paragraphs*).

aa. Regarding **claims 6, 15**:

bb. Yim appears to teach:

cc. the hardware state element comprises at least one from the group consisting of a processor register and a memory (*page 443, figure 3, CPU; since the element being emulated is a CPU, it would have been obvious that a hardware state element was a processor register*).

dd.Regarding **claims 7, 16**:

ee. Yim appears to teach:

ff. the high-level state element comprises at least one from the group consisting of a flip-flop, a latch, and a memory (*page 443, right-side column, first paragraph, "All the signals are characterized into three types: flip-flop, latch and combinational signal"*).

13. **Claims 8 and 17** are rejected under 35 U.S.C. 103(a) as being unpatentable over Yim as modified by Fischer and Ishtiaq as applied to claims **3 - 7 and 12 - 16** above, further in view of Dawson (Charles Dawson et al., "The Verilog Procedural Interface for the Verilog Hardware Description Language", 1996, Proceedings of the 1996 IEEE International Verilog HDL Conference, pages 17 - 23).

a. Yim as modified by Fischer and Ishtiaq teaches a method for providing verification for a simulation design as recited in claims **3 - 7 and 12 - 16** above.

b. The art of Dawson is directed to the programming language interface for Verilog.

c. The art of Dawson and the art of Yim as modified by Fischer and Ishtiaq are analogous art because they both are pertinent to the programming language interface for Verilog (*for example, see Yim, page 444, figure 6, programming language interface*).

d. Regarding **claims 8 and 17**:

e. Yim appears to teach:

f. the relationship comprises at least one of the group consisting of ~~a one-to-one relationship, a one-to-many relationship, and~~ a relationship defined by a mathematical function (*page 443, right-side column, first paragraph, "All the signals are characterized into three types: flip-flop, latch and combinational signal"; it would have been obvious that a combinational signal was a mathematical function*).

g. Yim does not specifically teach:

h. the relationship comprises at least one of the group consisting of a one-to-one relationship, a one-to-many relationship, ~~and a relationship defined by a mathematical function~~.

i. Dawson appears to teach:

j. the relationship comprises at least one of the group consisting of a one-to-one relationship, a one-to-many relationship (page 18, left-side column, section 2.1 Access methodology), ~~and a relationship defined by a mathematical function~~.

k. The motivation to use the art of Dawson with the art of Yim as modified by Fischer and Ishtiaq would have been the benefit recited I Dawson that the Verilog procedural interface provides a consistent data model of the complete Verilog HDL and an object oriented access to the data model (*page 18, left-side column, second paragraph*), which would have been recognized as a benefit by the ordinary artisan.

l. Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use the art of Dawson with the art of Yim as modified by Fischer and Ishtiaq to produce the claimed invention.

14. **Examiner's Note:** Examiner has cited particular columns and line numbers in the references applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the Applicant in preparing responses, to fully consider the references in their entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner. **The entire reference is considered to provide disclosure relating to the claimed invention**.

Conclusion

15. The prior art made of record and not relied upon is considered pertinent to the applicant's disclosure:

a. Tipon (U.S. Patent Number 5,859,962) teaches comparing detailed simulation results with high-level simulation results.

b. Court (U.S. Patent Number 5,438,673) teaches comparing detailed simulation results with high-level simulation results.

c. Bae (U.S. Patent Number 6,285,914) teaches comparing detailed simulation results with high-level simulation results.

d. Petsinger (U.S. Patent Number 6,625,759) teaches comparing reference model simulation results with behavioral simulation results.

e. Petsinger (U.S. Patent Number 7,139,936) teaches comparing reference model simulation results with behavioral simulation results.

f. Huggins (U.S. Patent Number 5,845,064) teaches comparing reference model simulation results with behavioral simulation results.

g. Chin (U.S. Patent Number 6,332,201) teaches comparing reference model simulation results with behavioral simulation results.

h. Cox (U.S. Patent 5,991,529) teaches inputting a test to a device and comparing the output results with expected results (*column 4, lines 39 - 55*).

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Russ Guill whose telephone number is 571-272-7955. The examiner can normally be reached on Monday - Friday 9:30 AM - 6:00 PM.

17. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez can be reached on 571-272-3753. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Any inquiry of a general nature or relating to the status of this application should be directed to the TC2100 Group Receptionist: 571-272-2100.

18. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Russ Guill
Examiner
Art Unit 2123

RG

ZOILA CABRERA
PRIMARY EXAMINER
TECHNOLOGY CENTER 2100
1/15/08